
# INTRODUCTION TO HPC
## MAELSTROM BOOTCAMP ECMWF

8 November 2023 | Dr. Andreas Herten | Forschungszentrum Jülich, MAELSTROM



MAELSTROM

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# Outline

# *What is* **HPC?**

**High Performance Computing** *is computing with a powerful machine using the available resources efficiently.*

*My interpretation.*

# Baseline

- What kind of CPU does your computer have?
  *CPU generation, clock ~~speed~~ rate, number of cores, vector length*

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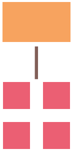



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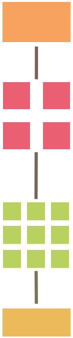

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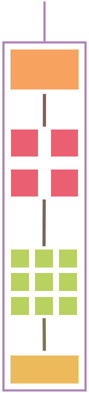



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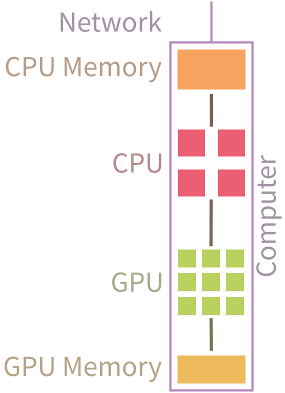
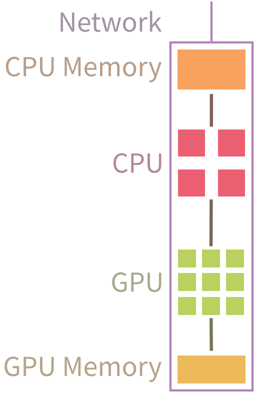
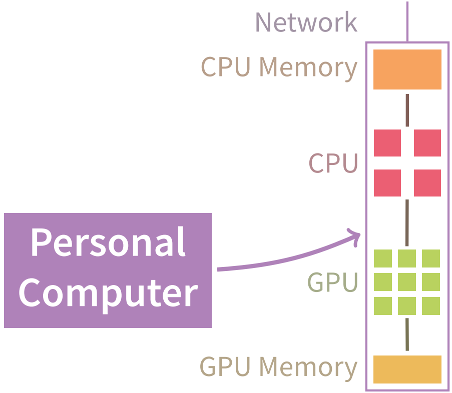



Network
CPU Memory
CPU
GPU
GPU Memory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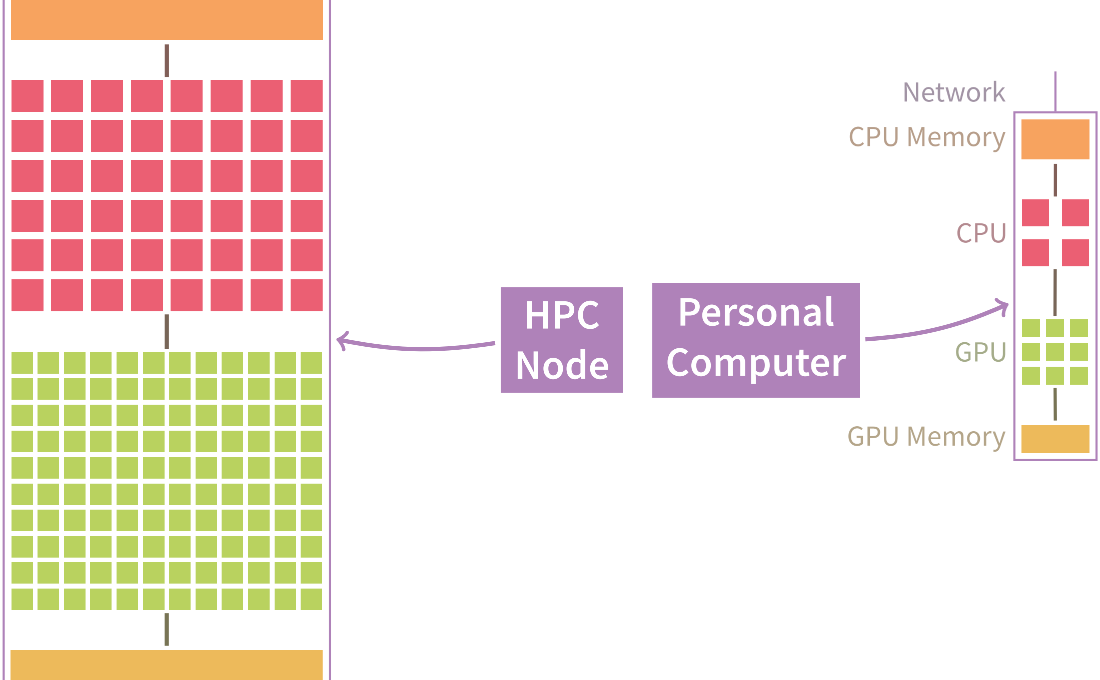
HPC Node
Personal Computer
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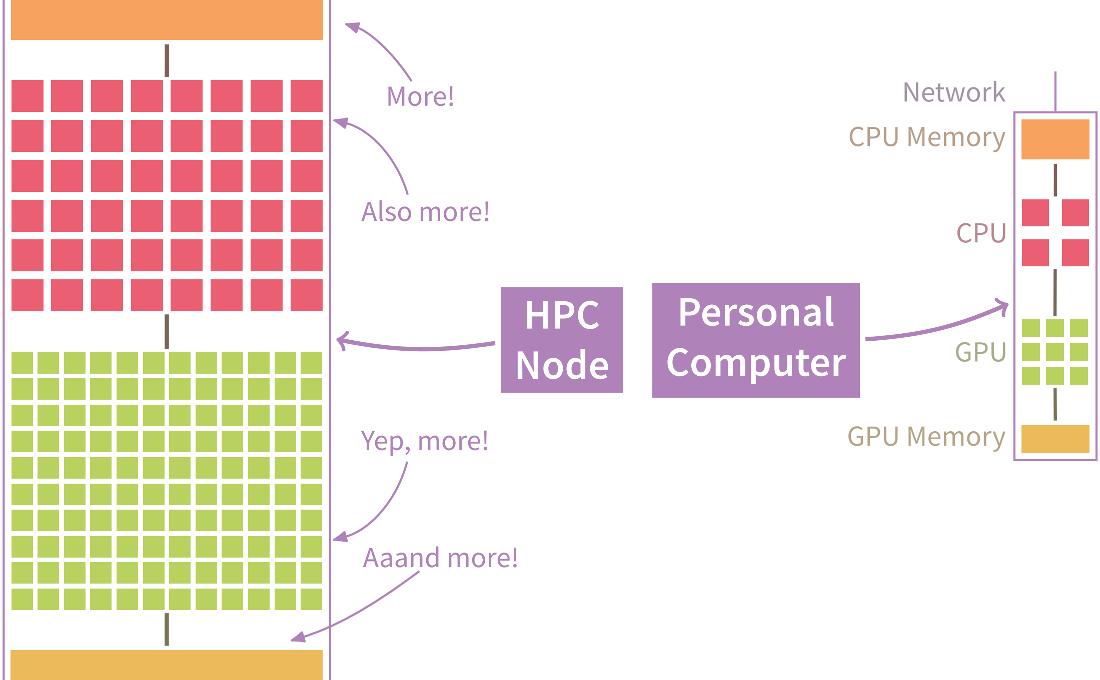

More!
Also more!
HPC Node
Personal Computer
Yep, more!
Aaand more!
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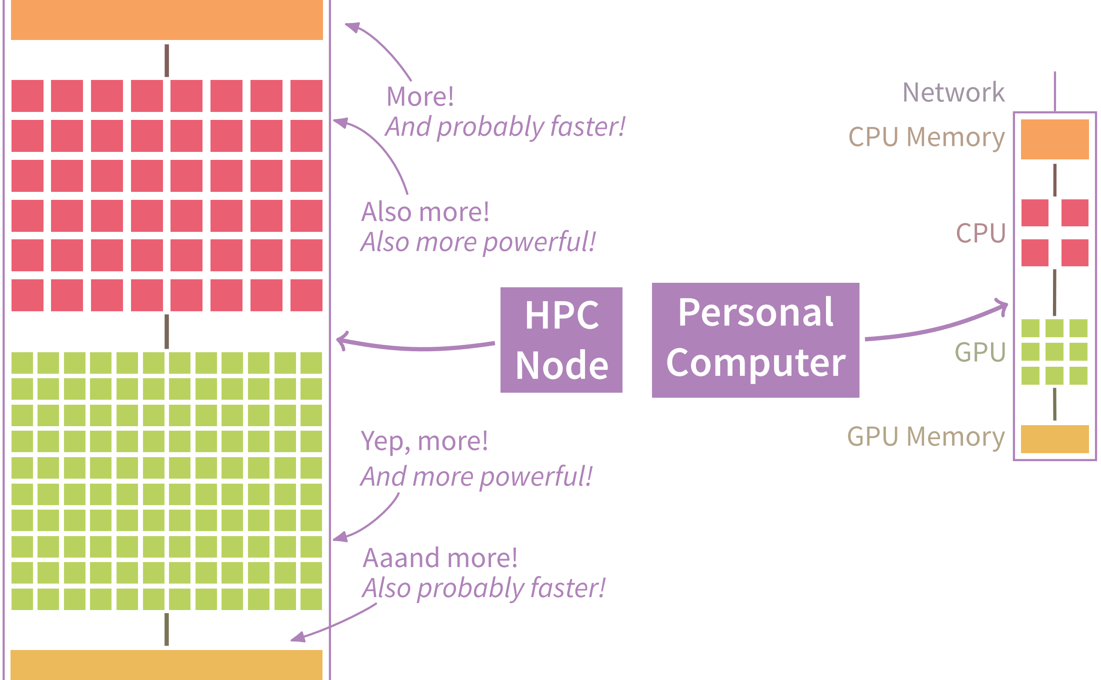
More!
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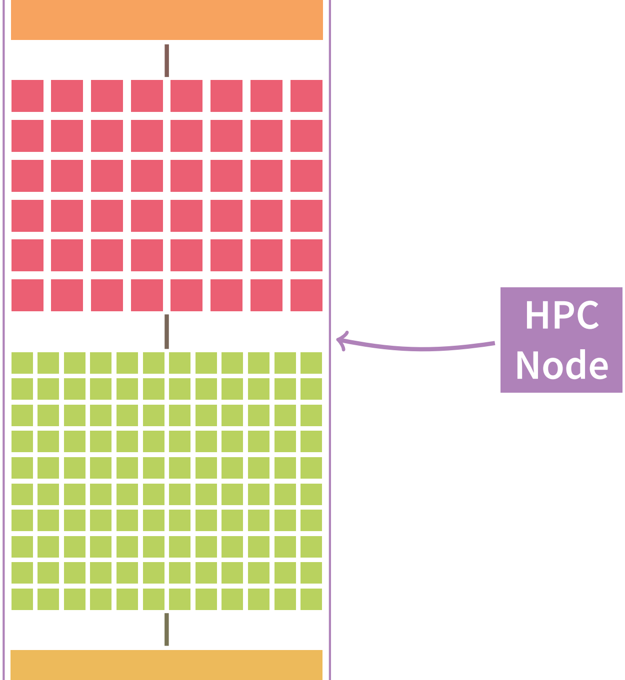
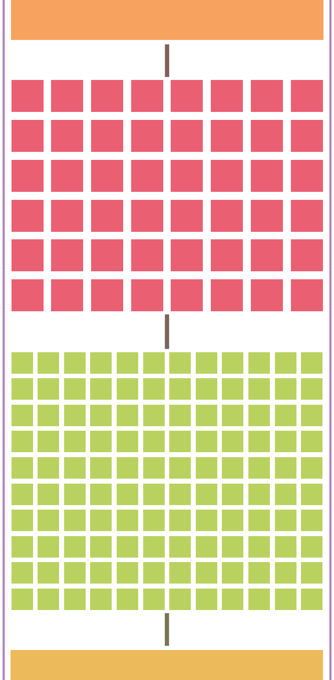
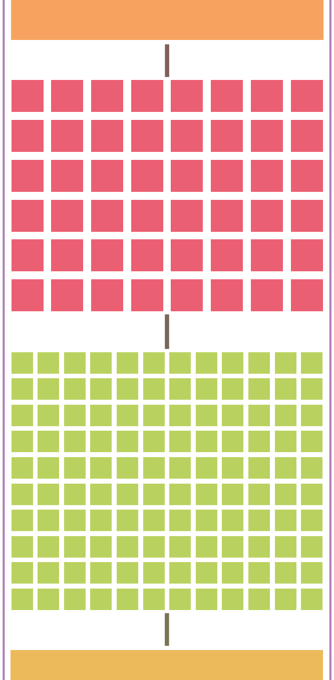

HPC
Node



CPU 64 cores, 2.2 GHz, 2× multi-threading, large caches, advanced instructions, 220 W TDP

**HPC Node**

*Specs based on JURECA DC*



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**Memory** 1 TB size, DDR4, 3200 MHz rate, 190 GiB/s bandwidth

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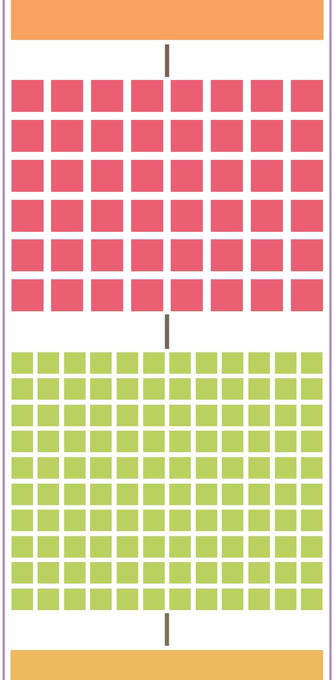

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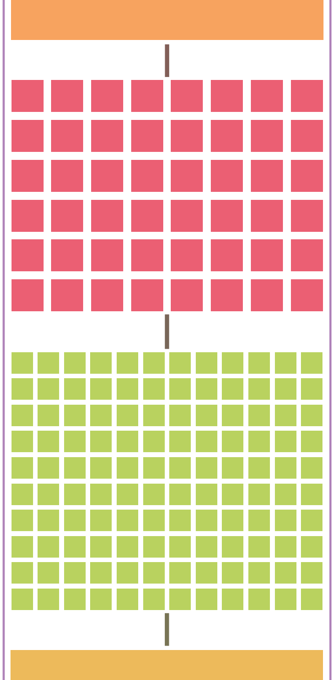

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GPU VRAM: 40 GB (80 GB also available), HBM2, 1.555 GB/s bandwidth

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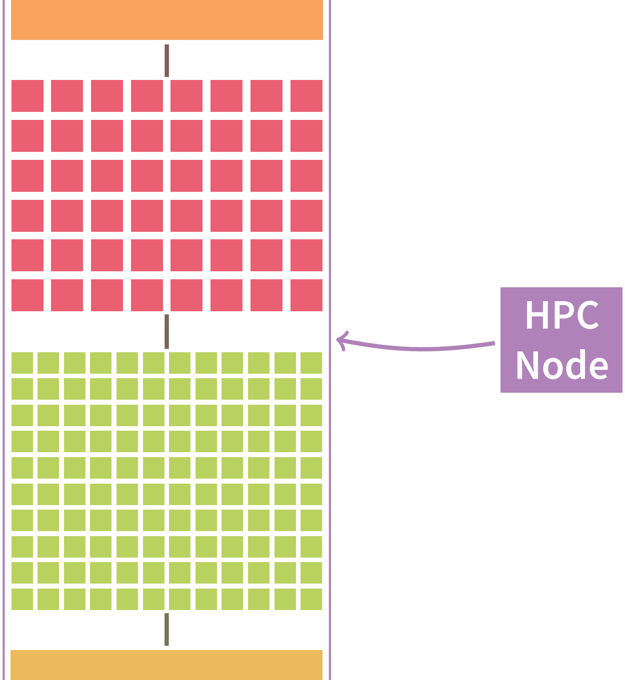
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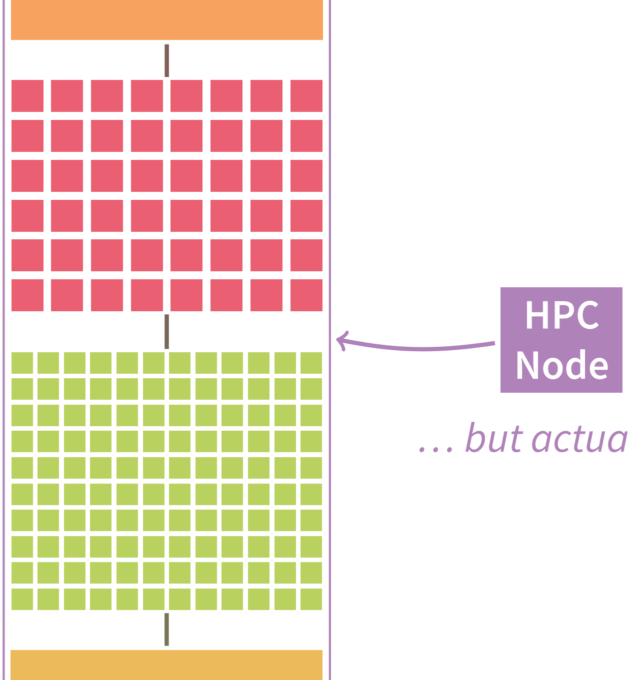
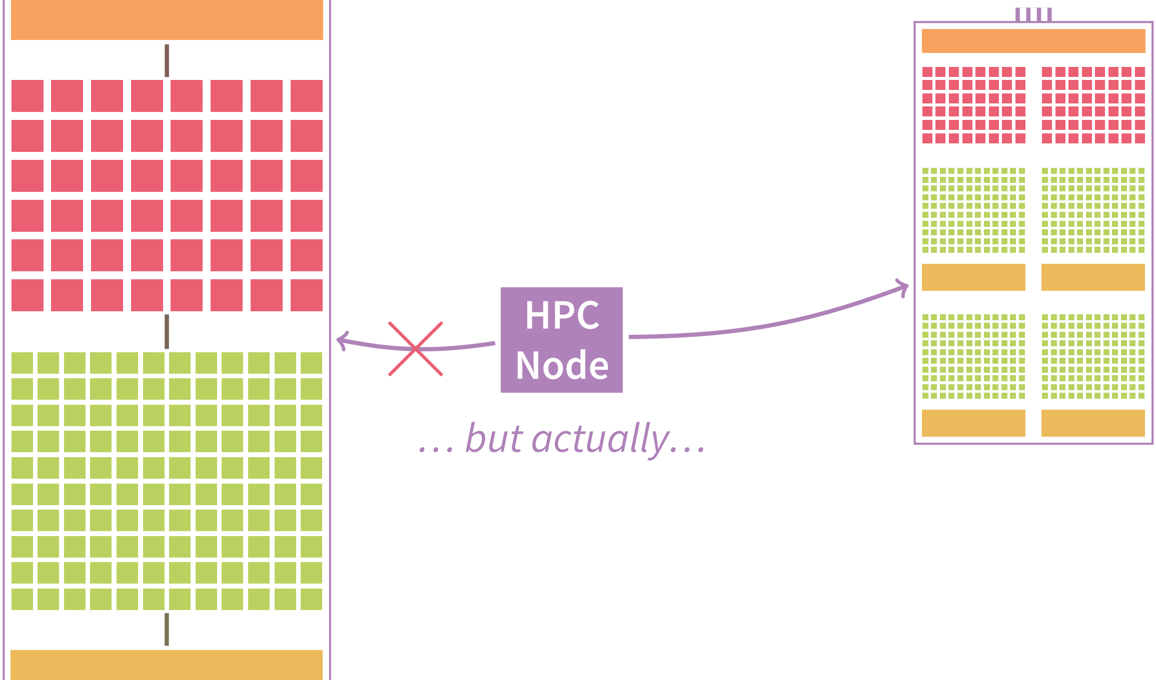



*… but actually…*


HPC
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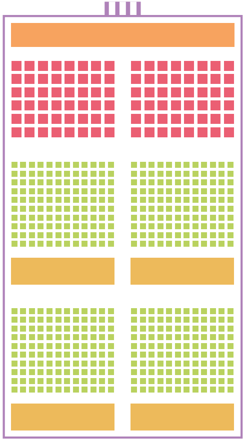
... but actually...

- Usually, 2 CPUs **sockets**, each with 64 cores; use mostly as one CPU with one memory
- 4 distinct GPUs, connected with each other (600 GB/s)
- 4 network connections, each 200 Gbit/s in each direction (*InfiniBand HDR-200*)

HPC Node



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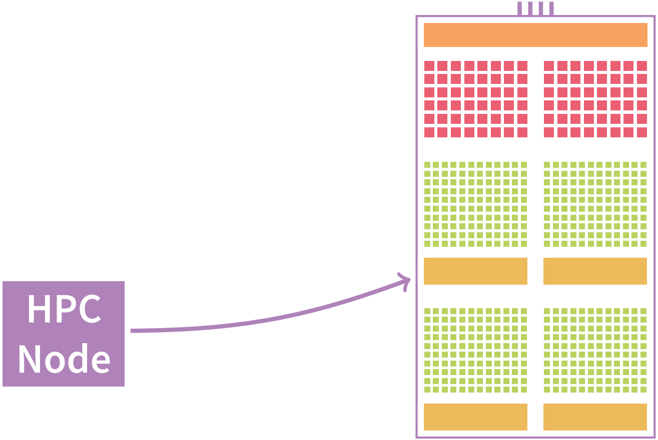


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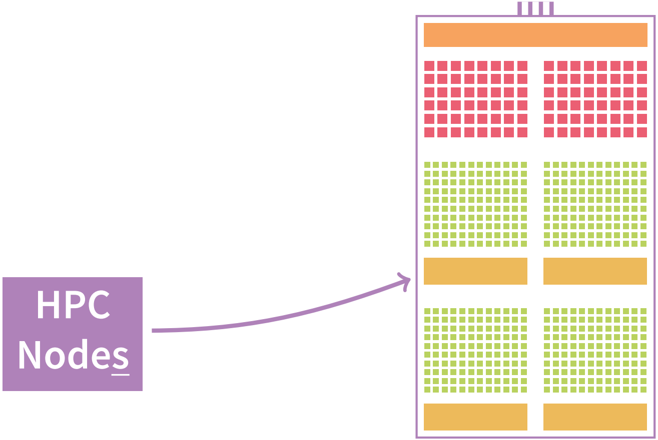


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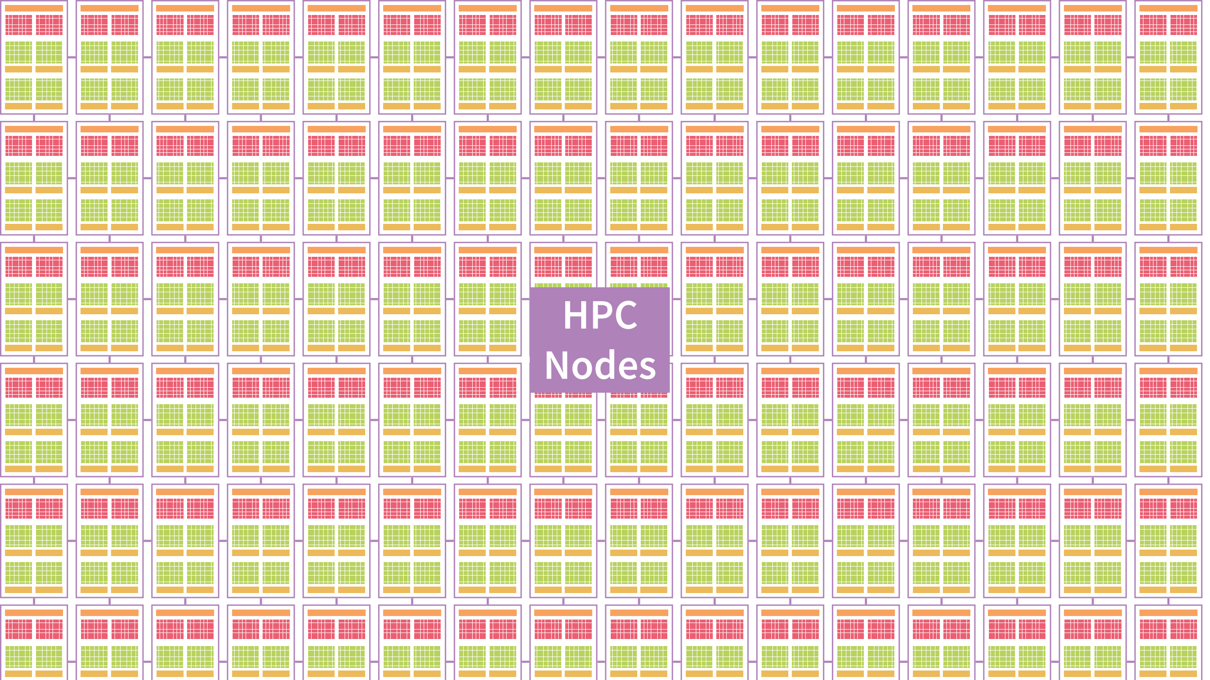
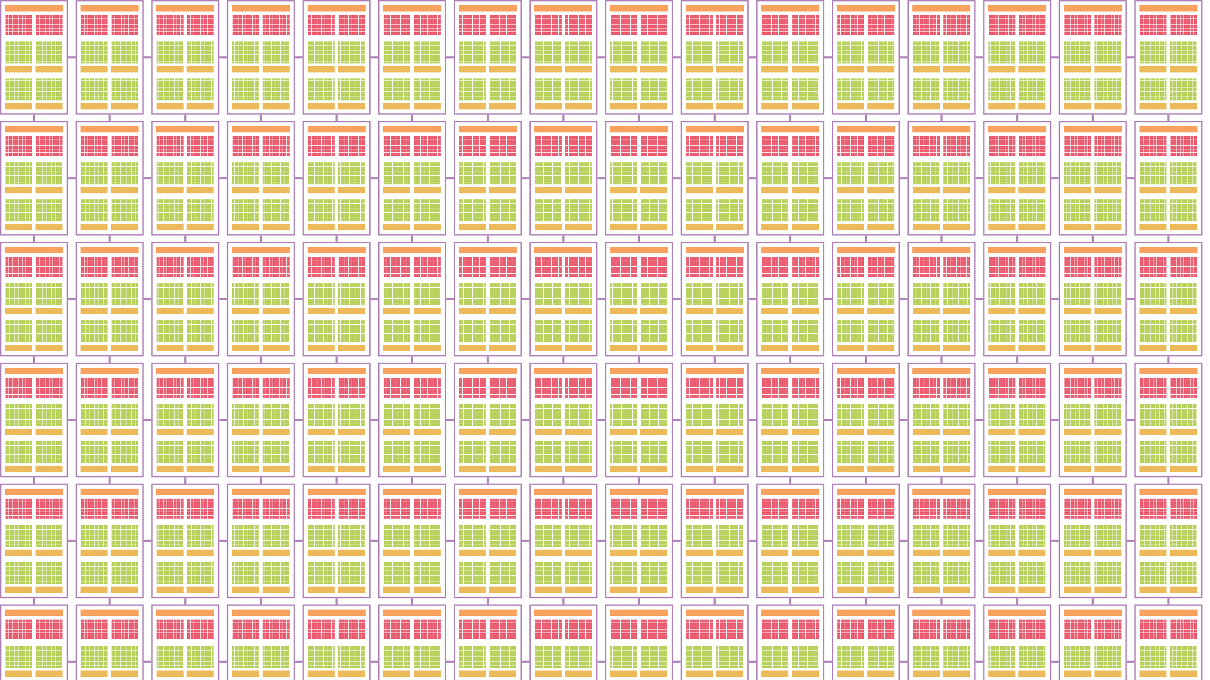
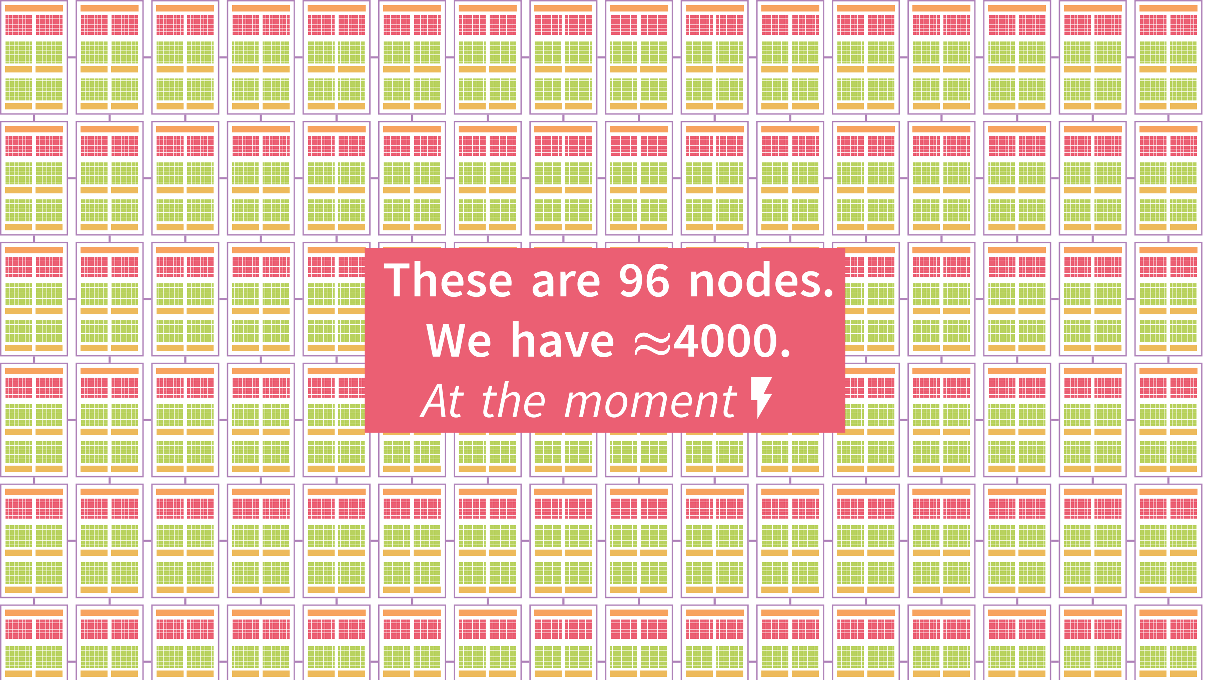

HPC
Nodes




These are 96 nodes.
We have ≈4000.
*At the moment*

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# Powerful Machines

Now

- Powerful nodes (large CPUs, accelerating GPUs, much memory)
- Many nodes (well-connected through high-speed interconnect)

→ **Beefed-up versions of commodity computers, with slight specializations; many**

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Past

- First computers: Supercomputers! Mainframe machines: Large installations with most powerful hardware at the time
- PC era: Even then, specialized computers, like vector machines, or many low-speed CPUs (well-connected)
- Recent history: x86, then PowerPC, then GPU accelerators, then specialized Arm CPUs

# Supercomputers in Pictures

- CDC 6600 supercomputer
- Around 1965
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- 3 MFLOP/S
- See Wikipedia for more
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HPC performance measured in **FLOP**/s.

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# Supercomputers in Pictures

- Cray-1 supercomputer
- Around 1978
- Very successful
- 160 MFLOP/S
- Probably pictured at NERSC

# Supercomputers in Pictures

- Intel XP/S 140 supercomputer
- Around 1994
- 3680 Intel i860 RISC processors; large-scale parallel system
- 143 GFLOP/s
- Picture by top500.org

# Supercomputers in Pictures


- JUGENE supercomputer
- 2008
- 294 912 PowerPC 450 cores; energy-efficient
- 800 TFLOP/s
- Picture by top500.org

# Supercomputers in Pictures


- Summit supercomputer
- 2018
- 27 000 GPUs hosted by POWER9 CPUs; first #1 GPU supercomputer
- 200 PFLOP/s
- Picture by Oak Ridge National Lab

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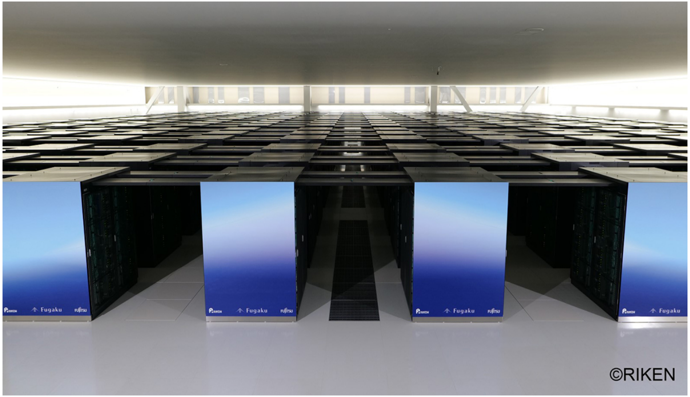


- Fugaku supercomputer
- 2020
- 7 630 848 Arm A64FX cores; #1 supercomputer at release
- 537 PFLOP/s
- Picture by RIKEN



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## JUWELS Cluster – Jülich's Scalable System

- 2500 nodes with Intel Xeon CPUs (2 × 24 cores)
- 46 + 10 nodes with 4 NVIDIA Tesla V100 cards (16 GB memory)
- 10.4 (CPU) + 1.6 (GPU) PFLOP/s peak performance (Top500: #86)



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## JUWELS Booster – Scaling Higher!

- 936 nodes with AMD EPYC Rome CPUs (2 × 24 cores)
- Each with 4 NVIDIA A100 Ampere GPUs (each: *FP64TC:* 19.5 / *FP64:* 9.7 TFLOP/s, 40 GB memory)
- InfiniBand DragonFly+ HDR-200 network; 4 × 200 Gbit/s per node


**Top500 List Nov 2021:**

- #1 Europe
- #8 World
- #4* Top/Green500

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# GPUs

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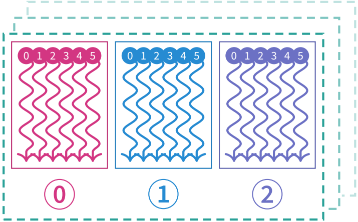

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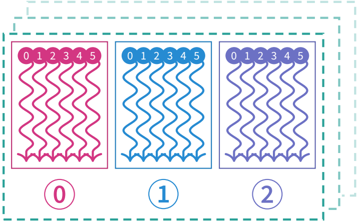

# GPUs


PCI Express 5.0 Host Interface
GigaThread Engine with MIG Control
GPC
TPC
SM
Memory Controller
HBM3
L2 Cache
L2 Cache
High-Speed Hub
NVLink

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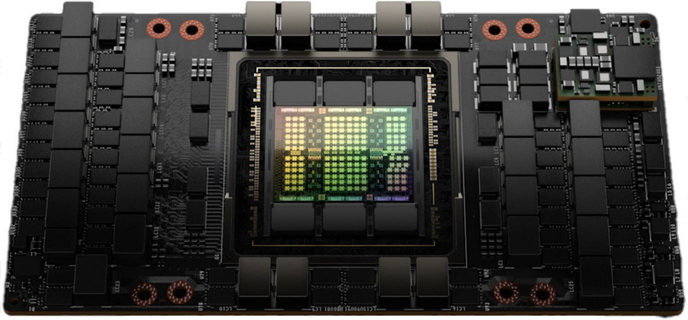

Picture by AMD [9]

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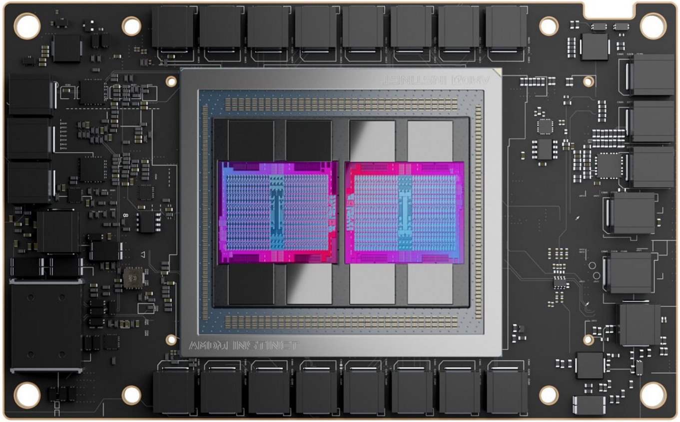


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2. Parallelize to all processing entities of node

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1. Exploit all capabilities of processing entity (*core*)
2. Parallelize to all processing entities of node
3. Distribute to all nodes



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# 1 Exploit All Capabilities of Processing Entity

- Modern CPUs: many advanced instructions, high clock rate, large caches, high memory bandwidth
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$+$ 4 additions
$=$ 4 assignments
$\rightarrow$ 8 instructions



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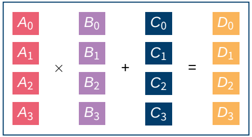


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SIMD $\longrightarrow$

$\times$ 1 multiplication
$+$ 1 addition
$=$ 1 assignment
$\rightarrow$ 2 instructions

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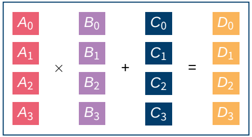


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\+ 4 additions
= 4 assignments
→ 8 instructions

SIMD →

× 1 multiplication
\+ 1 addition
= 1 assignment
→ 2 instructions

CPU Instruction: VADDPD

C Intrinsic: `_mm256_add_pd();`

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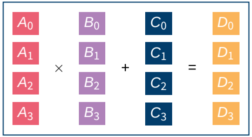


× 4 multiplications
+ 4 additions
= 4 assignments
→ 8 instructions

SIMD →

× 1 multiplication
+ 1 addition
= 1 assignment
→ 2 instructions

CPU Instruction: VADDPD

C Intrinsic: `_mm256_add_pd();`

FMA SIMD →

× 1 multiplication
+ 1 addition
= 1 assignment
→ **1 instruction**

# 1 Exploit All Capabilities of Processing Entity

- Modern CPUs: many advanced instructions, high clock rate, large caches, high memory bandwidth
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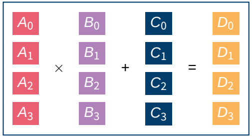


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CPU Instruction: VFMADD132PD

C Intrinsic: `_mm256_fmadd_pd;`



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- Example: Vectorization/SIMD

$$\begin{pmatrix} A_0 \\ A_1 \\ A_2 \\ A_3 \end{pmatrix} \times \begin{pmatrix} B_0 \\ B_1 \\ B_2 \\ B_3 \end{pmatrix} + \begin{pmatrix} C_0 \\ C_1 \\ C_2 \\ C_3 \end{pmatrix} = \begin{pmatrix} D_0 \\ D_1 \\ D_2 \\ D_3 \end{pmatrix}$$

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Compiler!

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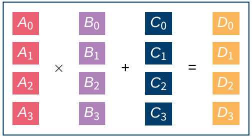


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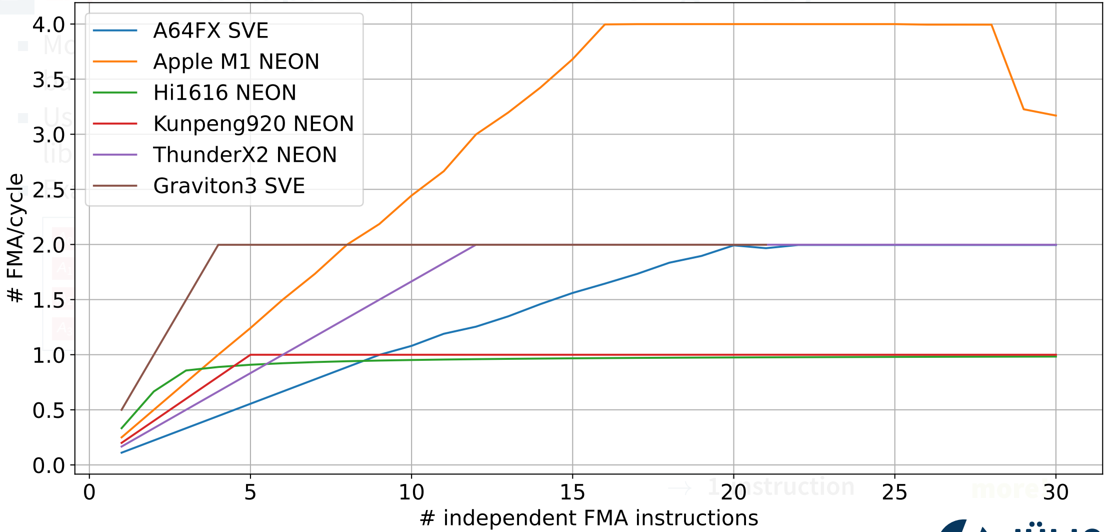
**Improve throughput!**

Compiler!

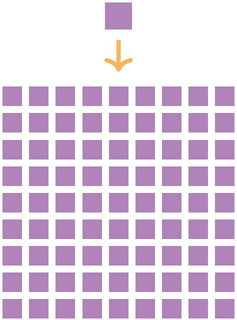
**Improve throughput more!**

*Analysis/plot by Stepan Nassyr, 2022.*



# 2 Parallelize to All Processing Entities of Node

- From core to cores



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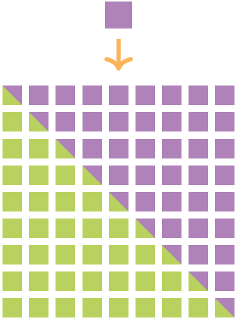
- From core to cores
- From CPU cores to GPU *cores*



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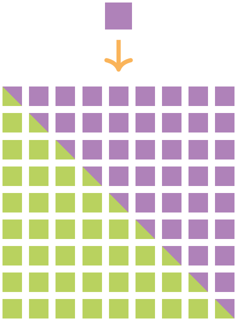
- **Parallelization**: Tasks work on portion of full problem using some local shared memory; *fine-grained* split



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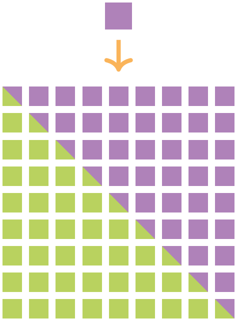
CPU Mostly through operating system capacities

  - OS *threads* launched on *cores*
  - Easiest threading interface: OpenMP

```
#pragma omp parallel for
for (int i = 0; i < N; i++) y[i] = x[i] * 3.14 + a[i];
```



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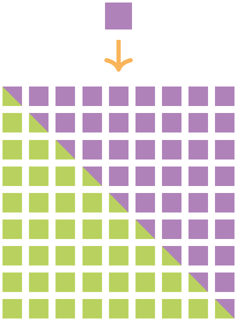
```

GPU Through dedicated programming environments

- Mostly, explicit models

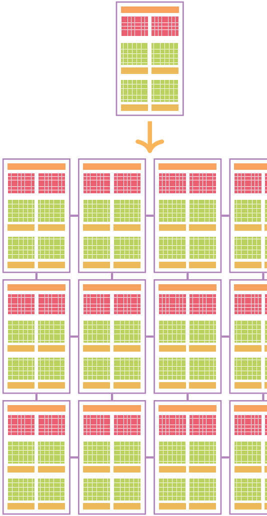
```
int i = threadIdx.x + blockIdx.x * blockDim.x;
y[i] = x[i] * 3.14 + a[i];
```

- Also, higher-level models (OpenMP, OpenACC)



# 3 Distribute to All Nodes

- From node to nodes



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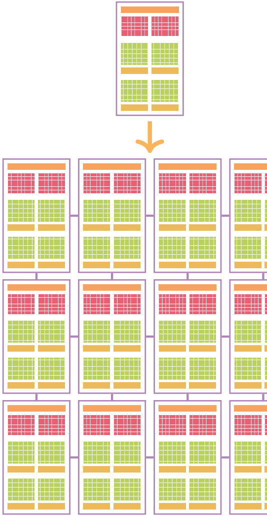

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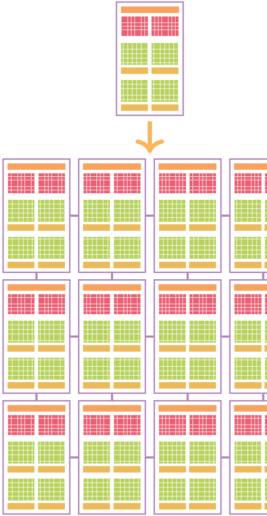
- Every task runs on own node with copy of program, defined exchange functions
- High-speed network important! GPUs directly attached to network



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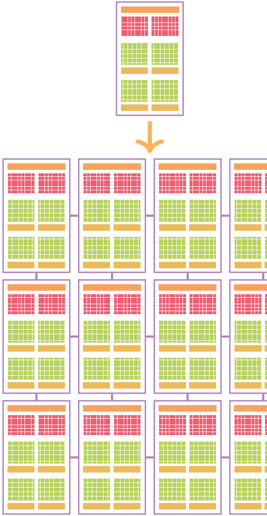
- Every task runs on own node with copy of program, defined exchange functions
- High-speed network important! GPUs directly attached to network
- Classical programming model: MPI

```
MPI_Comm_size(MPI_COMM_WORLD, &size);
MPI_Comm_rank(MPI_COMM_WORLD, &rank);
MPI_Send(buffer, 10, MPI_INT, 1, 555, MPI_COMM_WORLD);
MPI_Allreduce(local_sum, global_sum, 1, MPI_FLOAT, MPI_SUM,
↪   MPI_COMM_WORLD);
```





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# The Gateway Heroes of HPC

**Compilers** **Translate** high-level code to low-level machine code, with general *and* very architecture-specific optimizations

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| | |
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**Libraries** **Back-end**, low-level functions, usually optimized extensively, sometimes by vendors themselves

**Compilers**

- CPU: GCC, LLVM, Intel, Cray
- GPU: + NVIDIA CUDA, NVHPC, AMD
- Long history, constantly evolving

**Frameworks**

- MPI: OpenMPI, MPICH
- Threads: pthreads, OpenMP
- GPU: CUDA, HIP, SYCL, pSTL, Kokkos

**Libraries**

- CPU: MKL, BLIS, FFTW
- GPU: cuBLAS, rocBLAS, cuDNN
- → TensorFlow, PyTorch, ELPA

**High Performance Computing** *is* *computing with a powerful machine* *using the available resources efficiently.*

*My interpretation.*

# Conclusion

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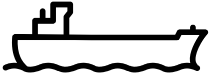
- HPC is intensive computing with largest machines
- Sometimes like Formula 1, sometimes like a tanker
- Sophisticated hardware is underlying everything, delivering up to 1.1 EFlop/s
- Advanced software holds everything together and enables science at the frontiers



Images by lastspark and Dmitry Podluzny from Noun Project.

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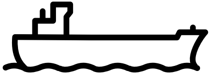

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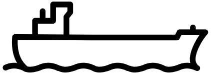

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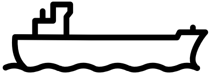
- We are hiring!
  `go.fzj.de/jsc-jobs`



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# Appendix

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# References: Images, Graphics I


[1] Forschungszentrum Jülich GmbH (Ralf-Uwe Limbach). *JUWELS Booster*.

[2] Control Data Corporation. *Picture: CDC 6600*. Computer History Museum. URL: `https://www.computerhistory.org/revolution/supercomputers/10/33` (pages 33, 34).

[3] Sandia National Lab. *Picture: Intel XP/S 140*. Top500.org. URL: `https://www.top500.org/resources/top-systems/intel-xps-140-paragon-sandia-national-labs/` (page 41).

[4] Forschungszentrum Jülich. *Picture: JUGENE*. JUGENE Press Release. URL: `https://www.fz-juelich.de/de/aktuelles/news/pressemitteilungen/2007/index4763_htm` (page 42).

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[5] OLCF at ORNL. *Picture: Summit*. Flickr. URL: https://www.flickr.com/photos/olcf/42659222181/ (page 43).

[6] RIKEN. *Picture: Fugaku*. Fujitsu.com. URL: https://blog.de.fujitsu.com/data-driven/fugaku-der-aktuell-weltweit-leistungsstaerkste-supercomputer/ (page 44).

[7] OLCF at ORNL. *Picture: Frontier*. Flickr. URL: https://www.flickr.com/photos/olcf/52117623843/.

[8] Nvidia Corporation. *Pictures: Ampere GPU*. Ampere Architecture Whitepaper. URL: http://www.nvidia.com/nvidia-ampere-architecture-whitepaper (pages 55–57).

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[9] AMD Inc. *Pictures: Instinct MI250 GPU*. Promotional Material. URL: `https://videocardz.net/amd-instinct-mi250` (page 58).



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